**Name – De Silva APC**

**Index – 210098R**

**Group – In21 CSE**

**Assigned Lab Task –**

Using the provided code and info, firstly designing a D flipflop and testing it via simulation. Then implementing the “Slow Clock” to obtain a slower clock that we need using the provided 100MHz clock of Basys board and then testing it via simulation. Finally designing the 3bit Counter that counts in the direction specified via an input using both slow clock and the d flipflops.

**Completed Truth Table -**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Qt | | | **Button**  **(B)** | **Qt+1** | | | **D2** | **D1** | **D0** |
| **Q2** | **Q1** | **Q0** | **Q2** | **Q1** | **Q0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

**Simplified Expressions for D0, D1 and D2  -**

**Diagram, engineering drawing

Description automatically generated**

**All VHDL Codes –**

***D\_FF.vhd***

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 04/08/2023 05:21:53 PM

-- Design Name:

-- Module Name: D\_FF - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity D\_FF is

Port ( D : in STD\_LOGIC;

Res : in STD\_LOGIC;

Clk : in STD\_LOGIC;

Q : out STD\_LOGIC;

Qbar : out STD\_LOGIC );

end D\_FF;

architecture Behavioral of D\_FF is

begin

process (Clk) begin

if (rising\_edge(Clk)) then

if Res = '1' then

Q <='0';

Qbar <= '1';

else

Q <= D;

Qbar <= not D;

end if;

end if;

end process;

end Behavioral;

***D\_FF\_Sim.vhd***

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 04/08/2023 05:33:01 PM

-- Design Name:

-- Module Name: D\_FF\_Sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity D\_FF\_Sim is

-- Port ( );

end D\_FF\_Sim;

architecture Behavioral of D\_FF\_Sim is

COMPONENT D\_FF

PORT( D,Res,Clk : IN STD\_LOGIC;

Q,Qbar : OUT STD\_LOGIC);

END COMPONENT;

SIGNAL D,Res,Clk : std\_logic;

SIGNAL Q,Qbar : std\_logic;

begin

UUT : D\_FF PORT MAP(

D => D,

Res => Res,

Clk => Clk,

Q => Q,

Qbar => Qbar

);

process

begin

D <= '0';

Res <= '0';

Clk <= '0';

WAIT FOR 100 ns;

D <= '1';

WAIT FOR 100 ns;

D <= '0';

Res <= '1';

WAIT FOR 100 ns;

D <= '1';

WAIT FOR 100 ns;

D <= '0';

Res <= '0';

WAIT FOR 30 ns;

Clk <= '1';

WAIT FOR 40 ns;

Clk <= '0';

WAIT FOR 30 ns;

D <= '1';

WAIT FOR 30 ns;

Clk <= '1';

WAIT FOR 40 NS;

Clk <= '0';

WAIT FOR 30 NS;

D <= '0';

Res <= '1';

WAIT FOR 30 ns;

Clk <= '1';

WAIT FOR 40 ns;

Clk <= '0';

WAIT FOR 30 ns;

D <= '1';

WAIT FOR 30 NS;

Clk <= '1';

WAIT FOR 40 NS;

Clk <= '0';

WAIT;

end process;

end Behavioral;

***Slow\_Clk.vhd***

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 04/08/2023 07:25:00 PM

-- Design Name:

-- Module Name: Slow\_Clk - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Slow\_Clk is

Port ( Clk\_in : in STD\_LOGIC;

Clk\_out : out STD\_LOGIC);

end Slow\_Clk;

architecture Behavioral of Slow\_Clk is

signal count : integer := 1;

signal clk\_status : std\_logic := '0';

begin

process (Clk\_in) begin

if(rising\_edge(Clk\_in)) then

count <= count+1;

if(count = 5)then -- Counting frequency scaler(Reduced to 5 to simulation purposes.IF not 5M.)

clk\_status <= not clk\_status;

Clk\_out <= clk\_status;

count<=1;

end if;

end if;

end process;

end Behavioral;

***Slow\_Clk\_Sim.vhd***

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 04/08/2023 07:30:53 PM

-- Design Name:

-- Module Name: Slow\_Clk\_Sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Slow\_Clk\_Sim is

-- Port ( );

end Slow\_Clk\_Sim;

architecture Behavioral of Slow\_Clk\_Sim is

COMPONENT Slow\_Clk

PORT( Clk\_in : IN STD\_LOGIC;

Clk\_out : OUT STD\_LOGIC);

END COMPONENT;

SIGNAL Clk\_in : std\_logic;

SIGNAL Clk\_out : std\_logic;

begin

UUT : Slow\_Clk PORT MAP(

Clk\_in => Clk\_in,

Clk\_out => Clk\_out

);

process

begin

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT FOR 10 ns;

Clk\_in <= '1';

WAIT FOR 10 ns;

Clk\_in <= '0';

WAIT;

end process;

end Behavioral;

***Counter.vhd***

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 04/08/2023 08:32:19 PM

-- Design Name:

-- Module Name: Counter - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Counter is

Port ( Dir : in STD\_LOGIC;

Res : in STD\_LOGIC;

Clk : in STD\_LOGIC;

Q : out STD\_LOGIC\_VECTOR (2 downto 0):="000");

end Counter;

architecture Behavioral of Counter is

component D\_FF

port (

D : in STD\_LOGIC;

Res: in STD\_LOGIC;

Clk : in STD\_LOGIC;

Q : out STD\_LOGIC;

Qbar : out STD\_LOGIC);

end component;

component Slow\_Clk

port (

Clk\_in : in STD\_LOGIC;

Clk\_out: out STD\_LOGIC);

end component;

signal D0, D1, D2 : std\_logic; -- Internal signals

signal Q0, Q1, Q2 : std\_logic; -- Internal signals

signal Clk\_slow : std\_logic; -- Internal clock

begin

Slow\_Clk0 : Slow\_Clk

port map (

Clk\_in => Clk,

Clk\_out => Clk\_slow);

D0 <= ((not Q2) and (not Dir)) or (Q1 and Dir);

D1 <= ((Q2 and Dir) or (Q0 and (not Dir)));

D2 <= (((not Q0)and Dir) or ((not Dir) and Q1));

D\_FF0 : D\_FF

port map (

D => D0,

Res => Res,

Clk => Clk\_slow,

Q => Q0);

D\_FF1 : D\_FF

port map (

D => D1,

Res => Res,

Clk => Clk\_slow,

Q => Q1);

D\_FF2 : D\_FF

port map (

D => D2,

Res => Res,

Clk => Clk\_slow,

Q => Q2);

Q(0) <= Q0;

Q(1) <= Q1;

Q(2) <= Q2;

end Behavioral;

***Counter\_sim.vhd***

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 04/08/2023 09:07:18 PM

-- Design Name:

-- Module Name: Counter\_sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Counter\_sim is

-- Port ( );

end Counter\_sim;

architecture Behavioral of Counter\_sim is

COMPONENT Counter

PORT( Dir,Res,Clk : IN STD\_LOGIC;

Q : OUT STD\_LOGIC\_VECTOR (2 downto 0));

END COMPONENT;

SIGNAL Dir,Res,Clk : std\_logic;

SIGNAL Q : std\_logic\_vector (2 downto 0);

begin

UUT : Counter PORT MAP(

Dir => Dir,

Res => Res,

Clk =>Clk,

Q =>Q

);

process

begin

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '0';

WAIT FOR 10 ns;

res <= '0';

dir <= '0';

Clk <= '1';

WAIT FOR 10 ns;

Clk <= '0';

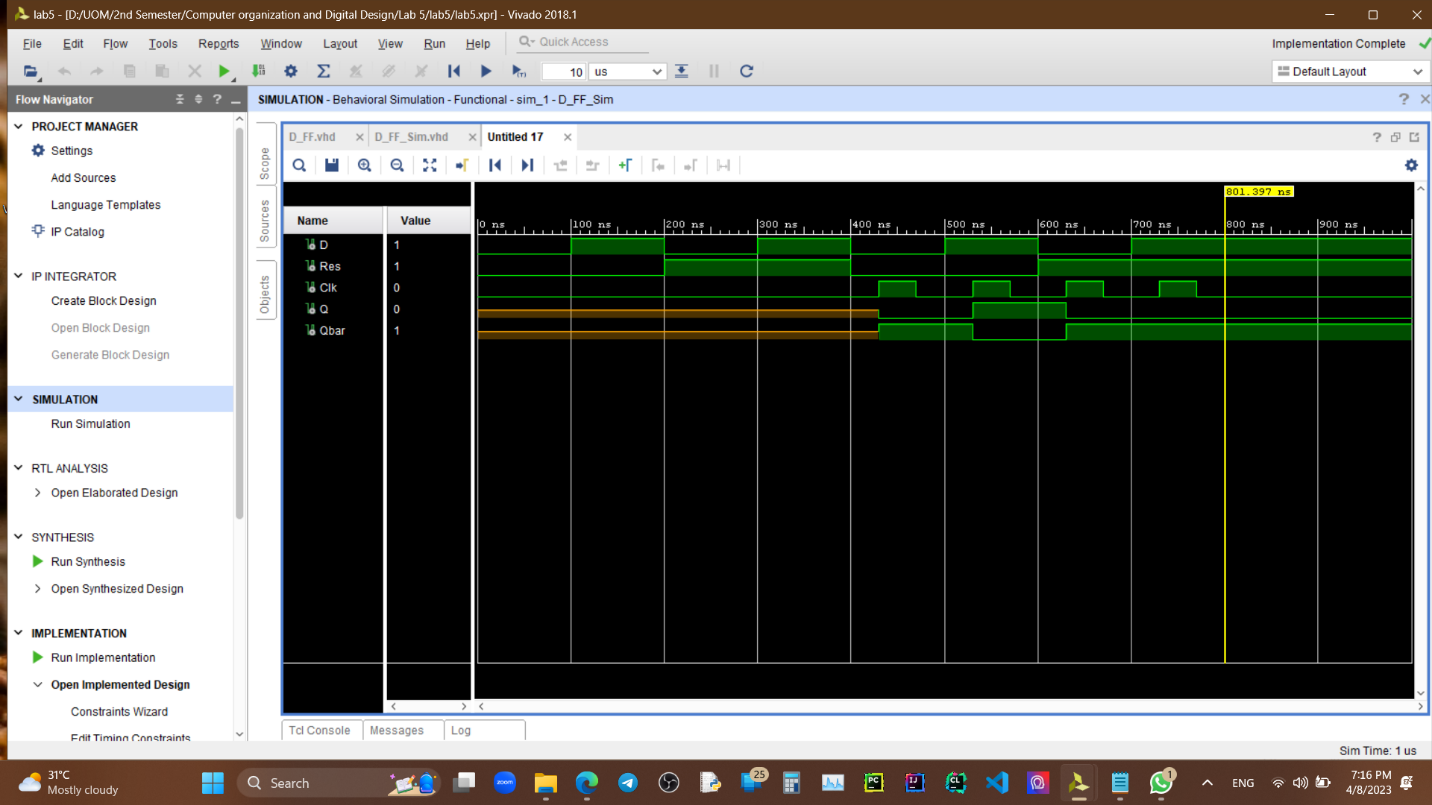
WAIT;

end process;

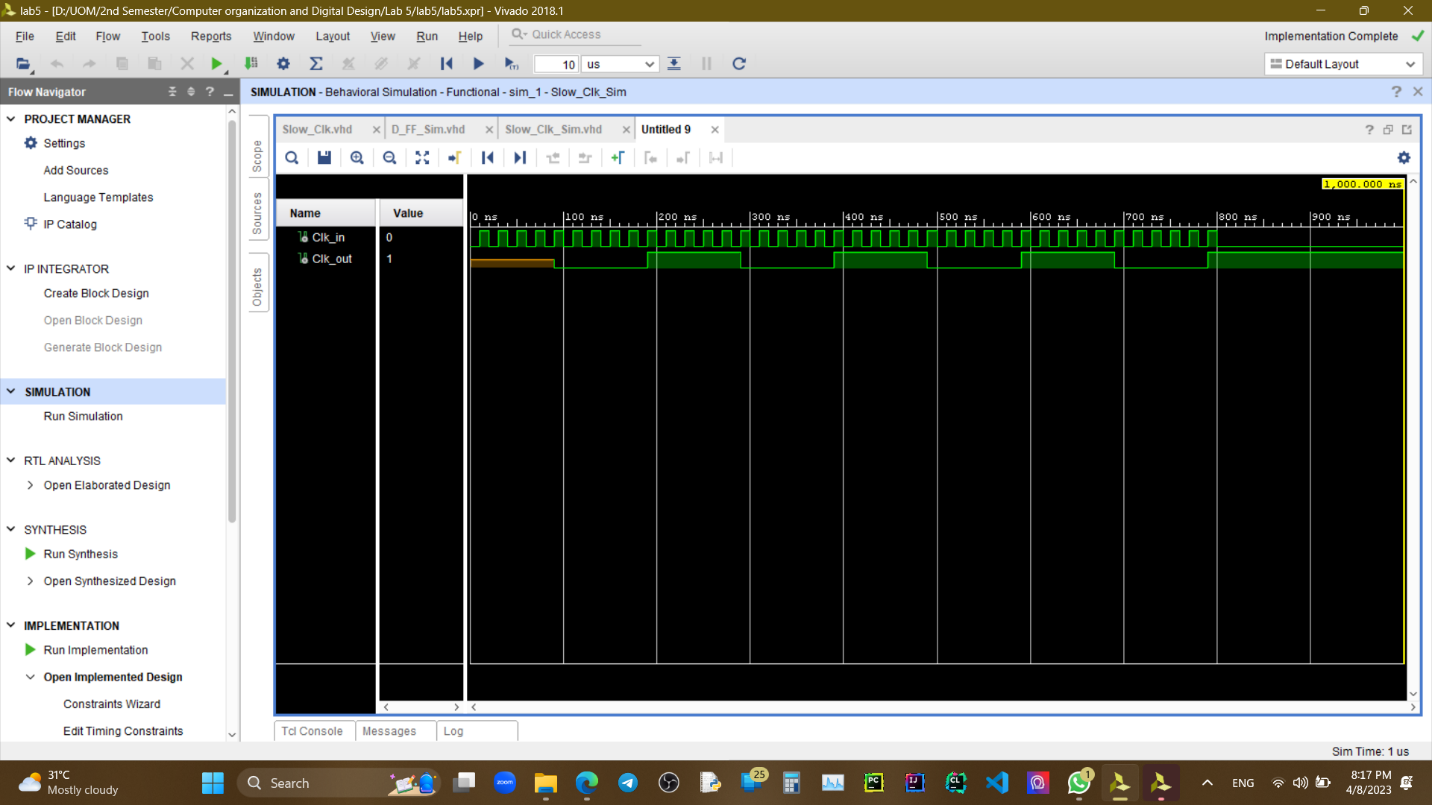
end Behavioral;

**Timing diagrams –**

***Simulating D Flip Flop –***

******

***Simulating Slow Clock –***

******

(Didn’t initialize any values for Q and Qbar in D flipflop and Clk\_out in Slow Clock explicitly) \*

***Counter (Failed) –***

***Graphical user interface, application

Description automatically generated***

**Conclusions –**

In conclusion, this lab exercise involved designing a D flip-flop and testing it via simulation. The next step was to implement a “Slow Clock” using the provided 100MHz clock of the Basys board and test it via simulation. Finally, a 3-bit counter was designed that counts in the direction specified via an input using both the slow clock and the D flip-flops. This exercise provided hands-on experience in designing and testing digital circuits using simulation tools. But sadly failed to successfully implement the final step, counter.